

WHAT IS CLAIMED IS:

1. A method for constructing a semiconductor device, the method comprising:

 forming a trench isolation structure and an active region proximate an outer surface of a semiconductor layer;

 depositing an epitaxial layer outwardly from the trench isolation structure;

 growing a first insulator layer outwardly from the epitaxial layer;

 growing a second insulator layer outwardly from the first insulator layer;

 forming a gate stack outwardly from the epitaxial layer, the gate stack comprising a portion of the first insulator layer, a portion of the second insulator layer, and a gate formed proximate the second insulator layer, the gate having a narrow region and a wide region; and

 heating the epitaxial layer to a temperature sufficient to allow for the epitaxial layer to form a source/drain implant region in the active region.

2. The method of Claim 1, wherein the trench isolation structure comprises silicon dioxide.

3. The method of Claim 1, wherein the epitaxial layer has a thickness of approximately 1,000 angstroms to 3,000 angstroms.

4. The method of Claim 1, wherein the epitaxial layer comprises silicon.

5. The method of Claim 1, wherein the epitaxial layer comprises silicon germanium.

6. The method of Claim 1, wherein the epitaxial layer comprises silicon germanium carbon.

7. The method of Claim 1, wherein the first insulator layer comprises silicon dioxide.

8. The method of Claim 1, wherein the second insulator layer comprises silicon nitride.

9. The method of Claim 1, wherein the gate stack comprises a third insulator layer formed outwardly from the second insulator layer, the third insulator layer comprising silicon dioxide.

10. The method of Claim 1, wherein forming the gate stack comprises:

etching the second insulator layer;

etching the first insulator layer to form a gate region;

growing a gate insulator layer outwardly from the gate region; and

forming the gate outwardly from the gate insulator layer.

11. The method of Claim 1, wherein forming the gate stack comprises:

etching the second insulator layer using a dry etching process;

etching the first insulator layer using a wet etching process to form a gate region;

growing a gate insulator layer outwardly from the gate region; and

forming the gate outwardly from the gate insulator layer.

12. The method of Claim 1, wherein:

a length of the narrow region of the gate is approximately one-tenth microns to two microns; and

a width of the narrow region of the gate is approximately 25 microns to 100 microns.

13. The method of Claim 1, wherein a length of the wide region of the gate is approximately two-tenths microns to two microns greater than a length of the narrow region of the gate.

14. A semiconductor device, comprising:

an outer surface of a semiconductor layer defining a trench isolation structure and an active region;

an epitaxial layer deposited outwardly from the trench isolation structure;

a first insulator layer grown outwardly from the epitaxial layer;

a second insulator layer grown outwardly from the first insulator layer;

a gate stack formed outwardly from the epitaxial layer, the gate stack comprising a portion of the first insulator layer, a portion of the second insulator layer, and a gate formed proximate the second insulator layer, the gate having a narrow region and a wide region; and

a source/drain implant region in the active region formed by heating the epitaxial layer to a temperature sufficient to allow for the epitaxial layer to form the source/drain implant region.

15. The semiconductor device of Claim 14, wherein the epitaxial layer has a thickness of approximately 1,000 angstroms to 3,000 angstroms.

16. The semiconductor device of Claim 14, wherein the epitaxial layer comprises silicon germanium carbon.

17. The semiconductor device of Claim 14, wherein the gate stack comprises a third insulator layer formed outwardly from the second insulator layer, the third insulator layer comprising silicon dioxide.

18. The semiconductor device of Claim 14, wherein:
a length of the narrow region of the gate is approximately one-tenth microns to two microns; and
a width of the narrow region of the gate is approximately 25 microns to 100 microns.

19. The semiconductor device of Claim 14, wherein a length of the wide region of the gate is approximately two-tenths microns to two microns greater than a length of the narrow region of the gate.

20. A semiconductor device, comprising:

an outer surface of a semiconductor layer forming a trench isolation structure and an active region, the trench isolation structure comprising silicon dioxide;

an epitaxial layer comprising silicon of a thickness of approximately 1,000 angstroms to 3,000 angstroms deposited outwardly from the trench isolation structure;

a first insulator layer comprising silicon dioxide grown outwardly from the epitaxial layer;

a second insulator layer comprising silicon nitride grown outwardly from the first insulator layer;

a third insulator layer comprising silicon dioxide formed outwardly from the second insulator layer;

a gate stack formed outwardly from the epitaxial layer, the gate stack comprising a portion of the first insulator layer, a portion of the second insulator layer, a portion of the third insulator layer, and a gate formed proximate the third insulator layer, the gate having a narrow region and a wide region, a length of the narrow region of the gate approximately one-tenth microns to two microns, a width of the narrow region of the gate approximately 25 microns to 100 microns, a length of the wide region of the gate approximately two-tenths microns to two microns greater than a length of the narrow region of the gate; and

a source/drain implant region in the active region formed by heating the epitaxial layer to a temperature sufficient to allow for the epitaxial layer to form the source/drain implant region.